ABSTRACT OF THE DISCLOSURE

A semiconductor device includes an alignment mark which is arranged adjacent to each corner of a semiconductor chip, and a plug which contacts the alignment mark. The alignment mark is formed by part of the uppermost interconnection layer in a multilevel interconnection which is formed on the semiconductor chip and obtained by stacking low-permittivity insulating layers and interconnection layers. The plug is buried in a contact hole formed in the low-permittivity insulating layer below the alignment mark, and contacts the alignment mark.